Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method of forming an SOI MOSFET device with a silicon layer formed on a dielectric layer with a gate electrode stack, with sidewall spacers on sidewalls of the gate electrode stack and raised source/drain regions formed on the surface of the silicon layer, wherein the gate electrode stack comprises a gate electrode formed of polysilicon over a gate dielectric layer formed on the surface of the silicon layer, comprising the steps of :
forming a cap layer over the gate electrode layer,
forming a gate mask for patterning the gate electrode over said polysilicon, said mask covering a portion of said cap layer, and said mask having a pattern and having a periphery,
etching the cap layer in the pattern of the gate mask with the etching process undercutting below said cap layer under the periphery of the mask thereby forming a notch in the cap layer below the mask,
patterning the electrode stack by etching in said pattern of said gate mask,
filling the notch with dielectric plugs between the gate polysilicon and the sidewall spacers for the purpose of eliminating the exposure of the gate polysilicon,

forming said sidewall spacers reaching along the sidewalls of the gate electrode to above the level where said plugs contact the gate polysilicon, and
forming a raised source region and a raised drain region on top of said silicon layer aside from said spacers, whereby formation of spurious epitaxial growth during the formation of raised source/drain regions is avoided.

[c2] The method of claim 1 wherein the cap layer comprises amorphous silicon formed by ion implantation of the polysilicon prior to forming the gate mask.

[c3] The method of claim 1 wherein said dielectric plugs and said sidewall spacers are formed by forming a blanket layer of a dielectric material which is etched back to form said plugs and said sidewall spacers.

[c4] The method of claim 2 wherein said dielectric plugs and said sidewall spacers are formed by forming a blanket layer of a dielectric material which is etched back to form said plugs and said sidewall spacers.

[c5] The method of claim 1 wherein
said gate mask comprises a hard mask, and
said cap layer comprises amorphous silicon formed by ion implantation of the polysilicon prior to forming the gate mask.

[c6] The method of claim 1 wherein
said gate mask comprises a hard mask, and
said dielectric plugs and said sidewall spacers are formed by forming a blanket layer of a dielectric material which is etched back to form said plugs and said side-wall spacers.

[c7] The method of claim 6 wherein said dielectric plugs and said sidewall spacers are formed by forming a blanket layer of a dielectric material which is etched back to form said plugs and said sidewall spacers.

[c8] The method of claim 1 wherein said cap layer is etched in the pattern of the mask. with a low pressure high bias etch forming said notch by said undercutting below said cap layer.

[c9] The method of claim 1 wherein
said cap layer is etched in the pattern of the mask. with a low pressure high bias etch forming said notch by said undercutting below said cap, and
then exposed surfaces of said cap layer are passivated by growing silicon oxide thereon.

[c10] The method of claim 1 wherein
said cap layer is etched in the pattern of the mask. with a low pressure high bias etch forming said notch by said

undercutting below said cap,
then exposed surfaces of said cap layer are passivated by growing silicon oxide thereon, and
then said polysilicon and said gate dielectric are etched in a highly selective RTE process in the pattern of said mask.

[c11] A method of forming an SOI MOSFET device with a silicon layer formed on a dielectric layer with a gate electrode stack, with sidewall spacers on sidewalls of the gate electrode stack and raised source/drain regions formed on the surface of the silicon layer, wherein the gate electrode stack comprises a gate electrode formed of polysilicon over a gate dielectric layer formed on the surface of the silicon layer, comprising the steps of :
forming a cap layer composed of amorphous silicon over the gate electrode layer,
forming a gate mask for patterning the gate electrode over said polysilicon, said mask covering a portion of said cap layer, and said mask having a pattern and having a periphery,
etching the cap layer in the pattern of the gate mask with the etching process undercutting below said cap layer under the periphery of the mask thereby forming a notch in the cap layer below the mask,
patterning the electrode stack by etching in said pattern

of said gate mask,
filling the notch with dielectric plugs between the gate polysilicon and the sidewall spacers for the purpose of eliminating the exposure of the gate polysilicon,
forming said sidewall spacers reaching along the sidewalls of the gate electrode to above the level where said plugs contact the gate polysilicon, and
forming a raised source region and a raised drain region on top of said silicon layer aside from said spacers, whereby formation of spurious epitaxial growth during the formation of raised source/drain regions is avoided.

[c12] The method of claim 11 wherein the amorphous silicon of said cap layer is formed by ion implantation of the polysilicon prior to forming the gate mask.

[c13] The method of claim 11 wherein said dielectric plugs and said sidewall spacers are formed by forming a blanket layer of a dielectric material which is etched back to form said plugs and said sidewall spacers.

[c14] The method of claim 12 wherein said dielectric plugs and said sidewall spacers are formed by forming a blanket layer of a dielectric material which is etched back to form said plugs and said sidewall spacers.

[c15] The method of claim 11 wherein

said gate mask comprises a hard mask, and
said cap layer comprises amorphous silicon formed by ion implantation of the polysilicon prior to forming the gate mask.

[c16] The method of claim 11 wherein
said gate mask comprises a hard mask, and
said dielectric plugs and said sidewall spacers are formed by forming a blanket layer of a dielectric material which is etched back to form said plugs and said side-wall spacers.

[c17] The method of claim 16 wherein said dielectric plugs and said sidewall spacers are formed by forming a blanket layer of a dielectric material which is etched back to form said plugs and said sidewall spacers.

[c18] The method of claim 11 wherein said cap layer is etched in the pattern of the mask. with a low pressure high bias etch forming said notch by said undercutting below said cap layer.

[c19] The method of claim 11 wherein
said cap layer is etched in the pattern of the mask. with a low pressure high bias etch forming said notch by said undercutting below said cap, and
then exposed surfaces of said cap layer are passivated

by growing silicon oxide thereon.

[c20] A SOI MOSFET device with a silicon layer formed on a dielectric layer with a gate electrode stack, with sidewall spacers on sidewalls of the gate electrode stack and raised source/drain regions formed on the surface of the silicon layer, wherein the gate electrode stack comprises a gate electrode formed of polysilicon over a gate dielectric layer formed on the surface of the silicon layer, comprising the steps of :

cap layer over the gate electrode layer,

a gate mask for patterning the gate electrode over said polysilicon, said mask covering a portion of said cap layer, and said mask having a pattern and having a periphery,

the cap layer being in the pattern of the gate mask with an undercut below said cap layer under the periphery of the mask in the form of a notch in the cap layer below the mask,

the notch being filled with dielectric plugs between the gate polysilicon and the sidewall spacers for the purpose of eliminating the exposure of the gate polysilicon,

said sidewall spacers reaching along the sidewalls of the gate electrode to above the level where said plugs contact the gate polysilicon, and

a raised source region and a raised drain region on top

of said silicon layer aside from said spacers.